Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in this Application.

1. (Currently amended) A method for making semiconductor device with an improved drive current, the semiconductor device having source and drain regions built on an active region, a length of the active region being different than a width thereof, comprising:

fabricating one or more isolation regions filled with an isolation material surrounding the active region;

annealing the isolation region[[,]] thereby shrinking ~~wherein~~ the isolation region ~~regions has~~ by at least 0.5% volume [[shrinkage after the annealing]], and compressing the isolation material wherein a stress caused by [[a]] the compression of the isolation material in the direction of the length of the active region is different from that caused by the compression of the isolation material in the direction of the width of the active region due to the difference between the width and the length.

2. (Original) The method of claim 1 wherein the fabricating further comprises filling the isolation regions with a porous isolation material.

3. (Original) The method of claim 2 wherein the porous isolation material is Ge based.

4. (Original) The method of claim 1 wherein the isolation material is deposited by a chemical vapor deposition with a TEOS based source material.

5. (Original) The method of claim 1 wherein the isolation material has an intrinsic tensile stress of at least 2.0E8 dynes per square centimeter.

6. (Original) The method of claim 1 further comprising:

forming a metal layer over the source or drain region; and

annealing the metal layer over the source or drain region to form a silicide.

7. (Original) The method of claim 6 wherein the silicide has an intrinsic stress larger than 2.0E8 dyne/cm^2.

8. (Original) The method of claim 6 wherein the silicide has a volume shrinkage larger than 10%.

9. (Original) The method of claim 6 wherein a thermal expansion mismatch between the source or drain region and the silicide is larger than 0.5% after being cooled down from annealing.

10. (Original) The method of claim 1 further comprising:

forming a gate electrode over the active region; and

forming at least one dielectric spacer adjacent to the gate electrode,

wherein the dielectric spacer has an intrinsic stress larger than 1.2E8 dyne/cm^2.

11. (Original) The method of claim 1 further comprising forming a contact etch stop layer over the device wherein the contact etch stop layer has its intrinsic stress modified to impose a stress that influences a net strain on the active region.

12. (Original) The method of claim 1 wherein the isolation regions has at least 8% volume shrinkage after the annealing.

13. (Withdrawn) A semiconductor device with an improved drive current, a length of the device being different from a width thereof, comprising:

one or more isolation regions filled with a predetermined isolation material surrounding the active region;

source and drain regions built on the active region;

a metal layer over the source and drain region to form a silicide; and

a gate electrode over the active region;

at least one dielectric spacer adjacent to the gate electrode; and

a contact etch stop layer over the device,

wherein the isolation regions has at least 0.5% volume shrinkage after the annealing so as to modulate a planar net strain on the active region, and

wherein the spacer and contact etch layer contribute to modulating a vertical net strain combined with the planar net strain so as to improve the drive current.

14. (Withdrawn) The device of claim 13 wherein the isolation material contains a porous isolation material.

15. (Withdrawn) The device of claim 14 wherein the porous isolation material is Ge.

16. (Withdrawn) The device of claim 13 wherein the isolation material has an intrinsic tensile stress of at lease 2.0E8 dynes per square centimeter.

17. (Withdrawn) The device of claim 13 wherein the silicide has an intrinsic stress larger than 2.0E8 dyne/cm^2.

18. (Withdrawn) The device of claim 13 wherein the silicide has a volume shrinkage larger than 10%.

19. (Withdrawn) The device of claim 13 wherein the silicide is such that a thermal expansion mismatch between the source or drain region and the silicide is larger than 0.5% during an annealing process.

20. (Withdrawn) The device of claim 19 wherein the thermal expansion mismatch is larger than 8%.

21. (Withdrawn) The device of claim 13 wherein the dielectric spacer has an intrinsic stress larger than 1.2E8 dyne/cm^2.

22. (Withdrawn) A method for making semiconductor device with an improved drive current, the semiconductor device having source and drain regions built on an active region, a length of the device being different than a width thereof, comprising:

fabricating one or more isolation regions surrounding the active region, the shape of the device is determined to be an "H" shape or a rectangle based on the width thereof;

filling the isolation regions with an predetermined isolation material whose volume shrinkage exceeds 0.5% after an anneal process;

forming a gate electrode over the active region;

forming one or more dielectric spacers next to the gate electrode;

forming an contact etch stopper layer over the device,

wherein the isolation regions, spacers and contact etch layer contribute to modulating a net strain imposed on the active region so as to improve the drive current.

23. (Withdrawn) The method of claim 22 further comprising:

forming a metal layer over the source and drain regions;

annealing the source and drain regions and metal layer to form silicide thereon, wherein the silicide has an intrinsic stress larger than 2.0E8 dyne/cm^2.

24. (Withdrawn) The method of claim 22 wherein the filling further comprises filling the isolation regions with a porous isolation material.

25. (Withdrawn) The method of claim 24 wherein the porous isolation material is Ge.

26. (Withdrawn) The method of claim 22 wherein the isolation material is deposited by a chemical vapor deposition with a TEOS based source material.

27. (Withdrawn) The method of claim 22 wherein the isolation material has an intrinsic tensile stress of at lease 2.0E8 dynes per square centimeter.

28. (Withdrawn) The method of claim 22 wherein the isolation material has a volume shrinkage exceeding 8% after the anneal process.

29. (Withdrawn) An N type semiconductor device with an improved drive current comprising an active region,

wherein atoms in the active region have a larger atomic distance in the direction parallel to a length of the active region than that in the direction parallel to a width of the active region.

30. (Withdrawn) A P type semiconductor device with an improved drive current comprising an active region,

wherein atoms in the active region have a larger atomic distance in the direction parallel to a width of the active region than that in the direction parallel to a length of the active region.

31. (New) The method as in claim 1, wherein the annealing causes atoms in the active region to have a different atomic distance in the direction parallel to the length of the active region than in the direction parallel to the width of the active region.

32. (New) The method as in claim 31, wherein the device is an N type semiconductor device and wherein the annealing causes atoms in the active region to have a larger atomic distance in the direction parallel to the length of the active region than that in the direction parallel to the width of the active region.